In the Claims:

The claims are as follows:

1. (Previously presented) A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of deep trenches, wherein forming each trench of the first plurality of deep trenches includes the steps of:

(i) providing a semiconductor substrate,

(ii) forming a hard mask layer on top of the semiconductor substrate,

(iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters,

(iv) etching a deep trench in the substrate via the hard mask opening; and

(b) determining a first yield of the first plurality of deep trenches; and

(c) if the first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a second set of etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches.

2. (Previously presented) The method of claim 1, further comprising the steps of,

determining a second yield of the second plurality of deep trenches; and

if the second yield of the second plurality of deep trenches is not within the pre-specified range of a target yield, forming a third plurality of deep trenches, wherein each trench of the third plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a third set of etching parameters, wherein the third set of etching parameters are adjusted from the second set of etching parameters such that, for each trench of the third plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the second plurality of deep trenches.

3. (Original) The method of claim 1, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, the step of etching the bottom portion of the hard mask opening has a lower degree of anisotropy than that associated with the a trench of the first plurality of deep trenches.

4. (Original) The method of claim 3, wherein the lower degree of anisotropy is achieved by reducing a flow rate of a noble gas.

5. (Original) The method of claim 4, wherein the noble gas comprises argon (Ar).

6. (Original) The method of claim 1, wherein the bottom portion of the hard mask opening has a greater lateral width than a top portion of the hard mask opening.

7. (Original) The method of claim 1,

wherein the step of forming the hard mask layer comprises the steps of:

forming a pad oxide layer on top of the semiconductor substrate, and

forming a nitride layer on top of the pad oxide layer,

wherein, in the formation of the first plurality of deep trenches, a first side wall of the bottom portion of the hard mask opening associated with the nitride layer has a first height,

wherein, in the formation of the second plurality of deep trenches, a second side wall of the bottom portion of the hard mask opening associated with the nitride layer has a second height, and

wherein the first height is greater than the second height.

8. (Original) The method of claim 7, wherein the step of forming the hard mask layer further comprises the steps of:

forming a BSG (borosilicate glass) layer on top of the nitride layer; and

forming an ARC (anti-reflective coating) layer on top of the BSG layer.

9. (Original) The method of claim 1, wherein the second set of etching parameters are further adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, the bottom portion of the hard mask opening has a rounder bottom corner than that corresponding to a trench of the first plurality of deep trenches.

10. (Original) The method of claim 9, wherein the rounder bottom corner is achieved by reducing a flow rate of a noble gas.

11. (Original) The method of claim 10, wherein the noble gas comprises argon (Ar).

12. (Original) The method of claim 1, wherein the step of etching the bottom portion of the hard mask opening comprises the steps of:

etching through a nitride layer of the hard mask layer; then

etching through an oxide layer of the hard mask layer; and then

etching through a portion of the semiconductor substrate.

13. (Original) The method of claim 12, further comprising the step of etching a top portion of the hard mask opening in a BSG layer and an ARC layer, wherein the top portion is above the bottom portion.

14. (Previously presented) A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming a hard mask layer on top of the semiconductor substrate;

(c) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening,

wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening such that a side wall of the bottom portion of the hard mask opening is substantially vertical, and such that the bottom portion of the hard mask opening has a greater lateral width than a top portion of the hard mask opening; and

(d) etching a deep trench in the substrate via the hard mask opening.

15. (Original) The method of claim 14, further comprising a de-polymerization step so as to remove polymers from a surface of the semiconductor structure after the step of etching the hard mask opening and before the step of etching the deep trench.

16. (Original) The method of claim 14, wherein the step of etching the bottom portion of the hard mask opening has a degree of anisotropy lower than a predetermined degree of anisotropy associated with a side wall angle which is considered substantially vertical.

17. (Canceled)

18. (Withdrawn) A semiconductor structure, comprising:

(a) a semiconductor substrate;

(b) a hard mask layer on top of the semiconductor substrate; and

(c) a hard mask layer opening in the hard mask layer,

wherein the semiconductor substrate is exposed to the atmosphere through the hard mask layer opening,

wherein the hard mask layer opening comprises top and bottom portions,

wherein the bottom portion is beneath the top portion, and

wherein a side wall of the bottom portion of the hard mask layer opening is substantially vertical.

19. (Withdrawn) The structure of claim 18, wherein the hard mask layer comprises:

a pad oxide on top of the semiconductor substrate; and

a nitride layer on top of the pad oxide layer,

wherein the nitride layer and the pad oxide layer are exposed to the atmosphere on a side wall of the bottom portion of the hard mask layer opening.

20. (Withdrawn) The structure of claim 18, wherein the bottom portion of the hard mask opening has a greater lateral width than the top portion of the hard mask opening.